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L7: (2) 6 and

L8: (1) 6 and

L6: (57) 5 ar

L9: (74) dram

L10: (74) 9 s

L11: (17) 10

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Search

DB: USPAT; US; PGPUB; EPD; JPO; DERWENT; IBM; TDB

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20020057446 A1	20020516	206	MULTI- INSTRUCTION STREAM PROCESSOR	358/1.13	358/1.15; 358/1.16;	
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20010021971 A1	20010913	252	SYSTEM FOR EXECUTING INSTRUCTIONS HAVING FLAG FOR	712/215		
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6414687 B1	20020702	201	Register setting-micro programming system	345/503	345/520; 345/559;	
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6393549 B1	20020521	132	Instruction alignment unit for routing variable	712/204	712/215	
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6393545 B1	20020521	201	Method apparatus and system for managing virtual memory	712/34	711/148; 711/153;	
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6349379 B1	20020219	201	System for executing instructions having flag for	712/210	712/225	
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6336180 B1	20020101	209	Method, apparatus and system for managing virtual memory	712/34	711/206; 711/207;	
8	<input type="checkbox"/>	<input type="checkbox"/>	US 6311258 B1	20011030	202	Data buffer apparatus and method for storing graphical	711/200	711/210; 711/211;	
9	<input type="checkbox"/>	<input type="checkbox"/>	US 6289138 B1	20010911	205	General image processor	382/307	382/308	
10	<input type="checkbox"/>	<input type="checkbox"/>	US 6272257 B1	20010807	301	Decoder of variable length codes	382/246		
11	<input type="checkbox"/>	<input type="checkbox"/>	US 6269436 B1	20010731	153	Superscalar microprocessor configured to predict return	712/23	712/228; 712/229;	

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Search:

DB: USPAT; US-PGPUS; EPO; JPO; DERWENT; IBM; 108

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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
12	<input type="checkbox"/>	<input type="checkbox"/>	US 6260073 B1	20010710	76	Network switch including a switch manager for	709/249	370/412; 370/911;	
13	<input type="checkbox"/>	<input type="checkbox"/>	US 6259456 B1	20010710	295	Data normalization techniques	345/619	345/501	
14	<input type="checkbox"/>	<input type="checkbox"/>	US 6246396 B1	20010612	299	Cached color conversion method and apparatus	345/604	345/549; 345/600;	
15	<input type="checkbox"/>	<input type="checkbox"/>	US 6237079 B1	20010522	239	Coprocessor interface having pending instructions queue	712/34	711/153	
16	<input type="checkbox"/>	<input type="checkbox"/>	US 6195674 B1	20010227	311	Fast DCT apparatus	708/402	708/401	
17	<input type="checkbox"/>	<input type="checkbox"/>	US 6189068 B1	20010213	142	Superscalar microprocessor employing a data cache	711/3	711/118; 711/204;	
18	<input type="checkbox"/>	<input type="checkbox"/>	US 6131140 A	20001010	24	Integrated cache memory with system control logic and	711/104	711/100; 711/118;	
19	<input type="checkbox"/>	<input type="checkbox"/>	US 6118724 A	20000912	211	Memory controller architecture	365/230.05	365/189.02; 365/221;	
20	<input type="checkbox"/>	<input type="checkbox"/>	US 6079006 A	20000620	152	Stride-based data address prediction structure	711/213	711/221; 712/237;	
21	<input type="checkbox"/>	<input type="checkbox"/>	US 6061749 A	20000509	324	Transformation of a first dataword received from a	710/65	345/603; 345/643;	
22	<input type="checkbox"/>	<input type="checkbox"/>	US 6014734 A	20000111	150	Superscalar microprocessor configured to predict return	712/23	712/228; 712/229;	

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☐ L7: (2) 6 anc
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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
34	<input type="checkbox"/>	<input type="checkbox"/>	US 5875315 A	19990223	180	Parallel and scalable instruction scanning unit	712/204		
35	<input type="checkbox"/>	<input type="checkbox"/>	US 5867723 A	19990202	62	Advanced massively parallel computer with a secondary	712/11	711/114; 711/119;	
36	<input type="checkbox"/>	<input type="checkbox"/>	US 5864707 A	19990126	149	Superscalar microprocessor configured to predict return	712/23	712/228; 712/243	
37	<input type="checkbox"/>	<input type="checkbox"/>	US 5860104 A	19990112	149	Data cache which speculatively updates a	711/137	711/126; 711/204;	
38	<input type="checkbox"/>	<input type="checkbox"/>	US 5859991 A	19990112	155	Parallel and scalable method for identifying valid	712/204		
39	<input type="checkbox"/>	<input type="checkbox"/>	US 5854921 A	19981229	145	Stride-based data address prediction structure	712/239	712/1; 712/23	
40	<input type="checkbox"/>	<input type="checkbox"/>	US 5848433 A	19981208	133	Way prediction unit and a method for operating the	711/137	711/118; 711/125;	
41	<input type="checkbox"/>	<input type="checkbox"/>	US 5832297 A	19981103	136	Superscalar microprocessor load/store unit employing a	710/5	710/56; 710/6;	
42	<input type="checkbox"/>	<input type="checkbox"/>	US 5832249 A	19981103	134	High performance superscalar alignment unit	712/204	712/215	
43	<input type="checkbox"/>	<input type="checkbox"/>	US 5826071 A	19981020	146	Parallel mask decoder and method for generating said	712/224	712/23	
44	<input type="checkbox"/>	<input type="checkbox"/>	US 5822574 A	19981013	131	Functional unit with a pointer for mispredicted	712/233	712/215; 712/217;	

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as well as interfacing to other buses such as peripheral bus. The present invention also provides for improved layout of a cache array with a data path logic management unit as well as power management features for the cache array and a tag RAM with comparator on, in one embodiment, the same chip with the cache array or on an associated chip in another embodiment.



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output terminals 32 and 34. The write access interface 26, under control of the control interface 24, provides for buffering, queuing and routing of data for storage in the RAM core 28, the data being communicated to the memory circuit 22 at one or more of the data input terminals 32. The read access interface 30, under control of the control interface 24, provides for routing, queuing and buffering of data stored in the RAM core 28 for communication at one or more of the data output terminals 34.

Detailed Description Text - DETX (12):

The memory circuit 36 shown in FIG. 3 is a specific embodiment of the memory circuit 22 shown generally in FIG. 2. In memory circuit 36, the control interface 24 comprises a master control 40, a load control 42, a RAM access control 44, and an unload control 46. The control interface 24, as shown, also comprises a refresh control 48. The refresh control 48 is employed when the

United States Patent [19] **Patent** [11]
McAlpine [45] **Date of**

[54] **HIGH PERFORMANCE DIGITAL ELECTRONIC SYSTEM ARCHITECTURE AND MEMORY CIRCUIT THEREFOR** [57]
A digital electronic system components communicating data digital electronic system control bus, coupled means and to the memory control signals and memory circuit is provided of the ports (i) having terminal that transfer operating independently coupled respectively for data communication memory array is provided read from a row of placing in the queue size of the block and interface preferably selection circuit preferably selectable blocks of positions in selected array is also provided he written to the array the array a contiguous block and its placement preferably comprises circuit preferably is able data received from selectable positions

[76] **Inventor:** Gary L. McAlpine, 11555 SW 155th Ter., Beaverton, Oreg. 97007

[21] **Appl. No.:** 09/035,640

[22] **Filed:** Mar. 5, 1998

Related U.S. Application Data

[62] **Division of application No.** 08/612,376, Mar. 5, 1997, Pat. No. 5,802,582, which is a continuation of application No. 08/300,421, Sep. 1, 1994, abandoned.

[51] **Int. Cl.:** G06F 12/02

[52] **U.S. Cl.:** 711/149; 711/143; 711/146

[56] **Field of Search:** 711/131, 149, 711/168, 143, 146

[56] **References Cited**

U.S. PATENT DOCUMENTS

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5,440,523 8/1995 Jaffe 365/236.05

Primary Examiner—Hiep T. Nguyen

20 Clm

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Taylor	[45] Date of Patent:	Dec. 1, 1998
[54] DUAL PORT MEMORIES AND SYSTEMS AND METHODS USING THE SAME	5,390,139 2/1993 Smith	365/29
	5,368,431 10/1990 Rao	365/189.12
	5,621,502 4/1997 Cases et al.	355/309
[73] Inventor: Ronald T. Taylor, Grapevine, Tex.	5,636,174 6/1997 Rao	365/230.03
	5,649,101 7/1997 Andrade et al.	365/494
[73] Assignee: Citrus Logic, Inc., Fremont, Calif.	5,687,132 11/1997 Rao	365/230.03
[21] Appl. No.: 666,813	Primary Examiner—David Nelms	
[23] Filed: Jun. 19, 1996	Assistant Examiner—Hos V. Ho	
[51] Int. Cl. ⁶ G11C 8/00	Attorney, Agent, or Firm—James J. Murphy; Steven A. Shaw	
[52] U.S. Cl. 365/230.05; 365/230.03		
[56] Field of Search 365/230.05, 230.03, 355/220		
[57] ABSTRACT		
	A memory 20 includes a first array 100 and a second array 102 of memory cells. A first data port 118 allows for the exchange of data with the first array 100 and a second data port 120 allows for the exchange of data with the second array 102. Memory system 20 also includes a circuitry 122 for controlling data exchanges in a selected mode with the first array 100 via the first data port 118 and with the second array 102 via the second data port 120, the exchanges with the first and second arrays 100 and 102 being asynchronous.	
[58] References Cited		
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22 Claims, 4 Drawing Sheets		

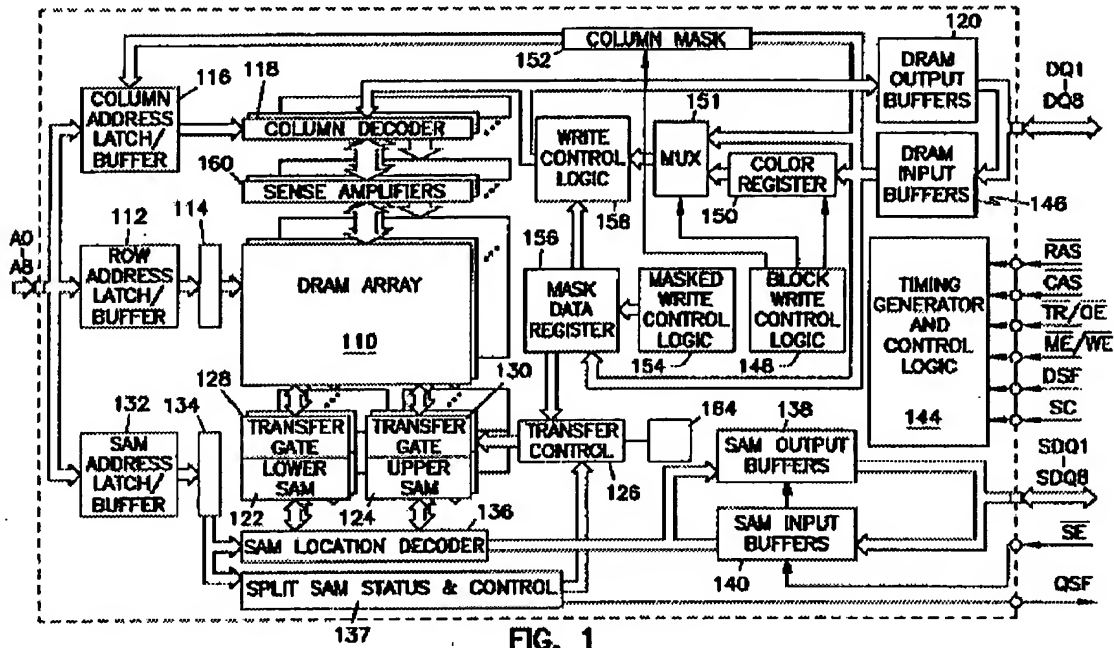


FIG. 1

U.S. Patent

Aug. 12, 1997

Sheet 1 of 13

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